Transactional Memory

How to live without locks.

Till Smejkal

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TECHNISCHE UNIVERSITÄT DRESDEN

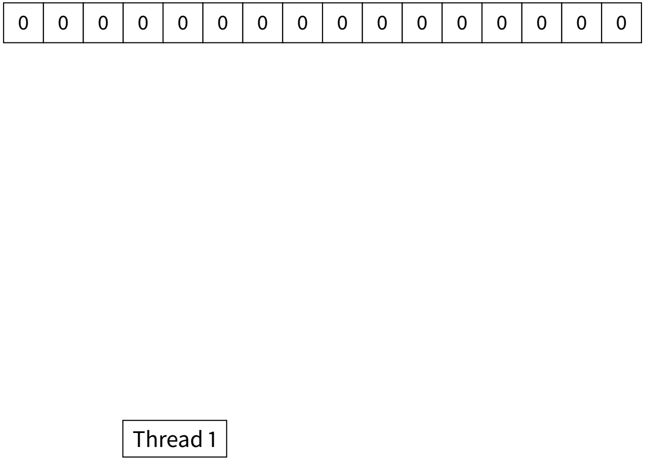
Motivation

```
int data[SIZE];

void thread_fn(int cnt) {
    /* initialize random */

    for (int i = 0; i < cnt; ++i) {
        auto pos = rand();
        data[pos]++;
    }
}
```

Motivation

0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Motivation



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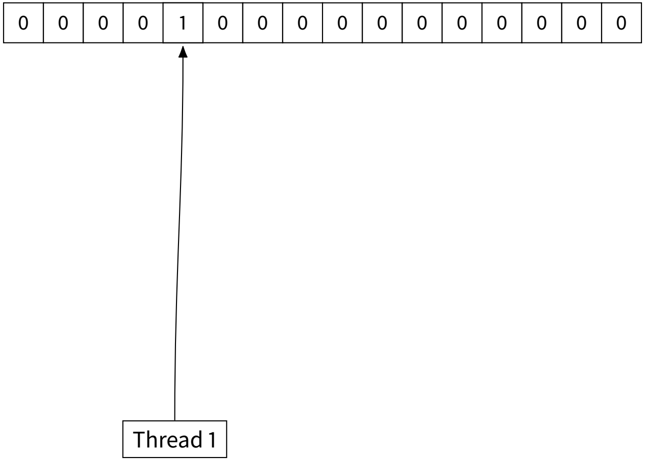

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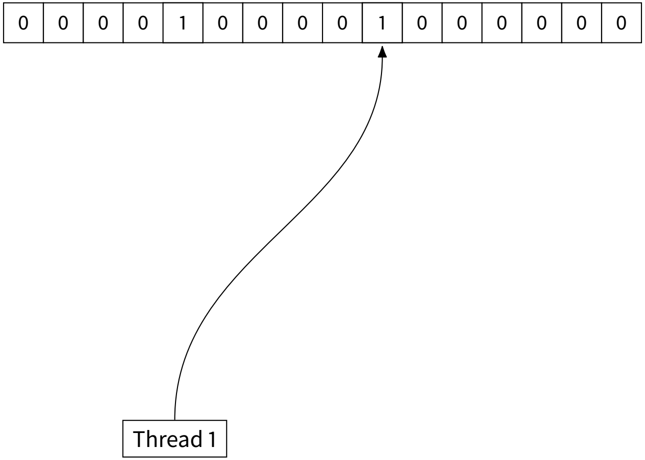

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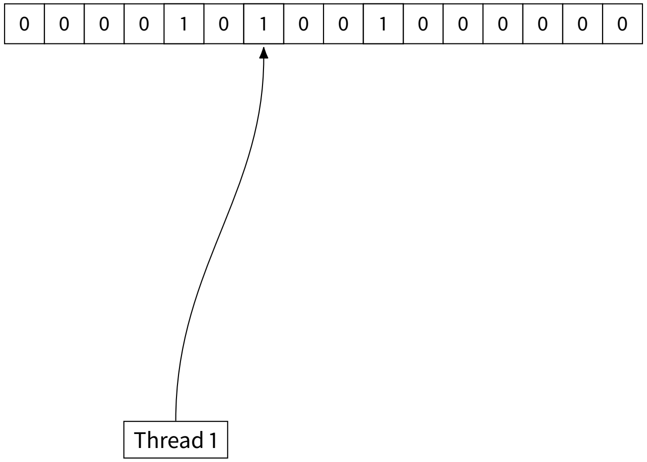

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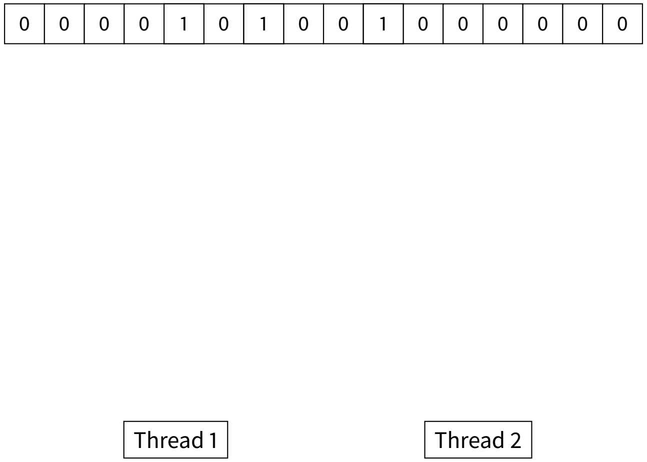

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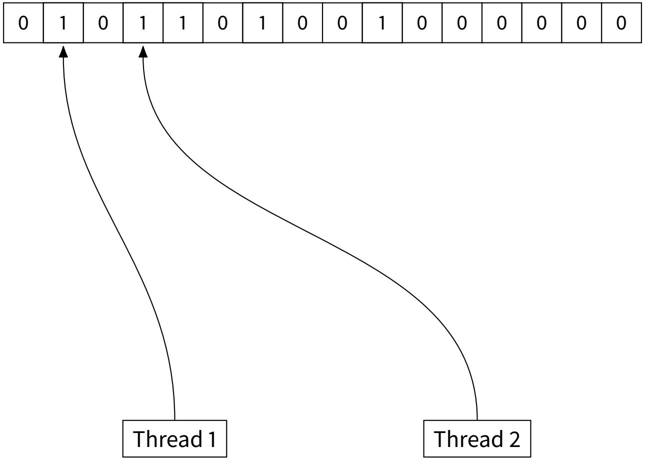

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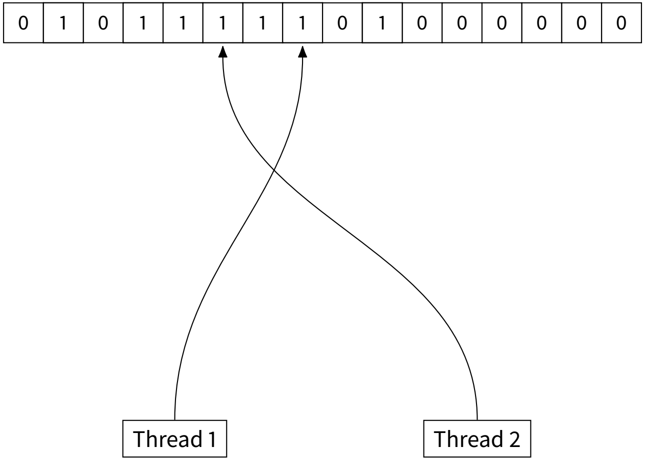

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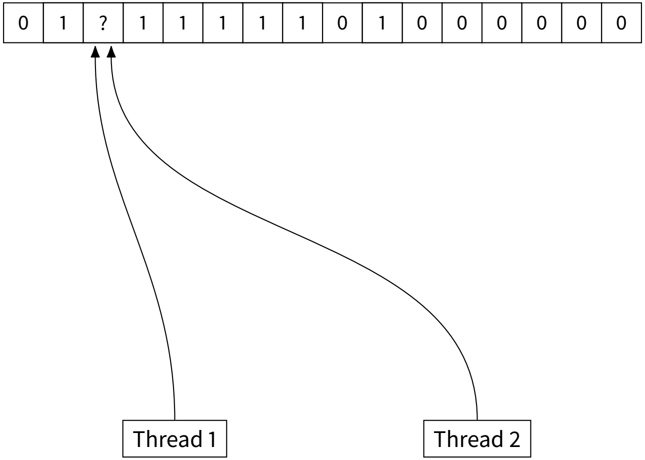

Motivation
Coarse Locking

```
int data[SIZE];
std::mutex mtx;

void thread_fn(int cnt) {
    /* initialize random */

    for (int i = 0; i < cnt; ++i) {
        auto pos = rand();

        mtx.lock();
        data[pos]++;
        mtx.unlock();
    }
}
```

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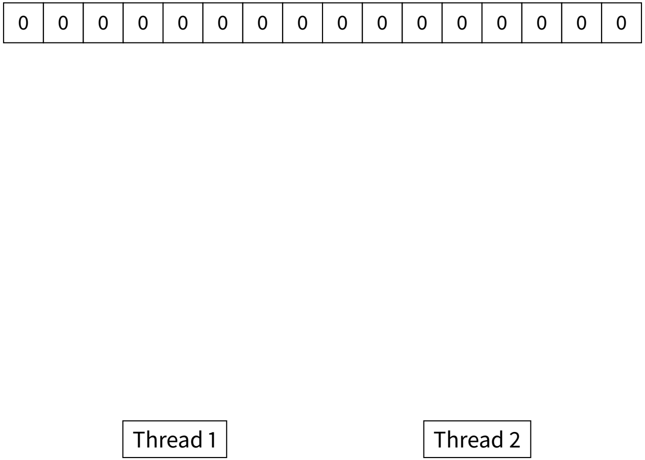
Coarse Locking



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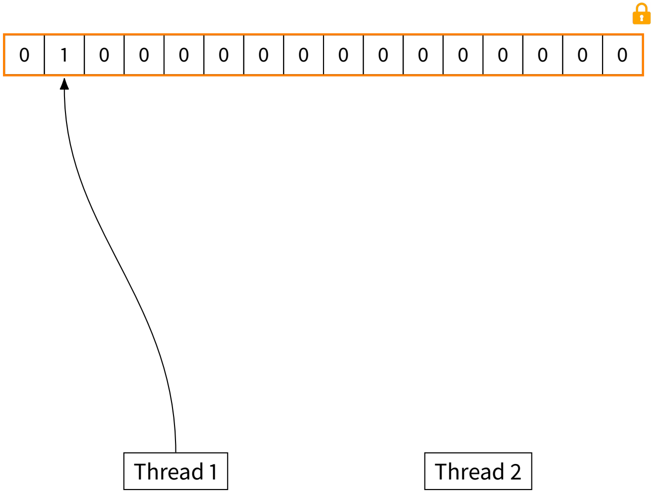

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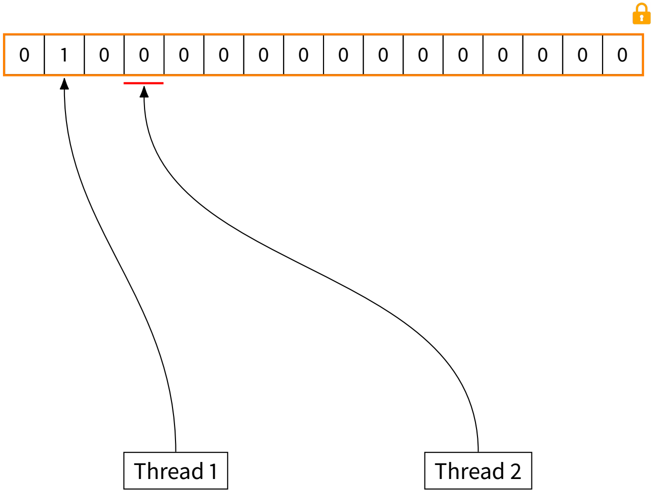

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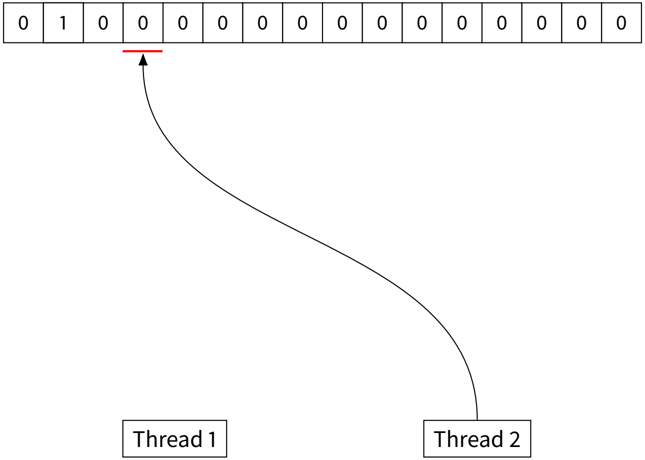

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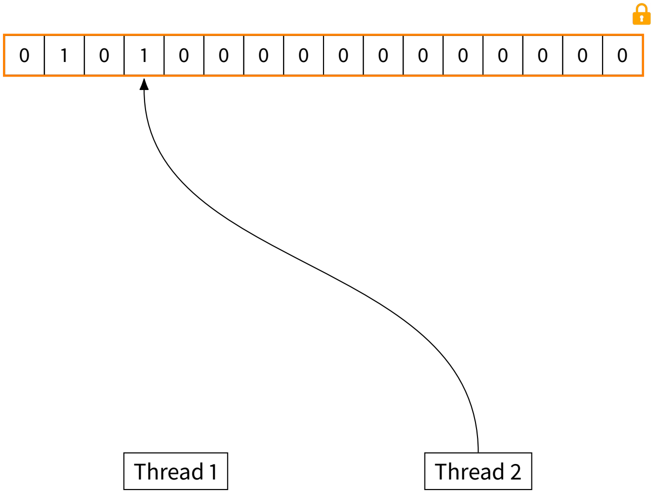

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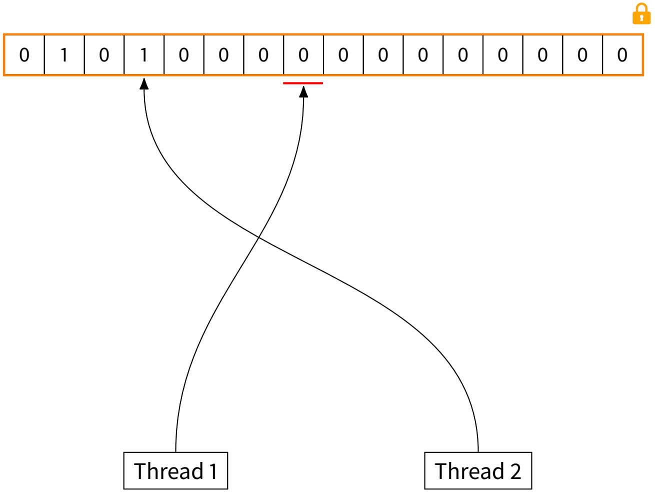

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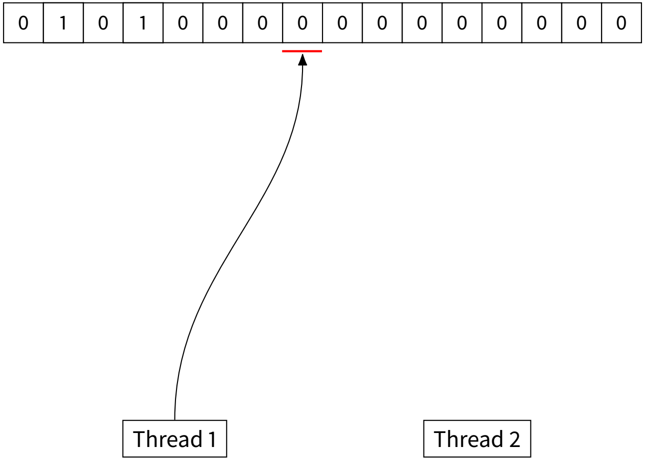

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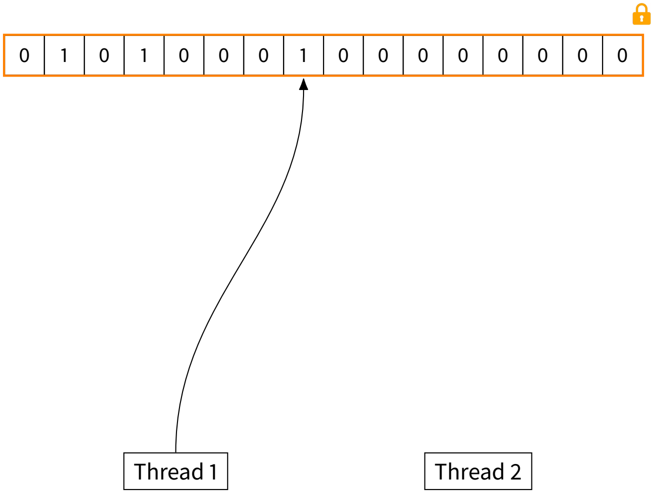

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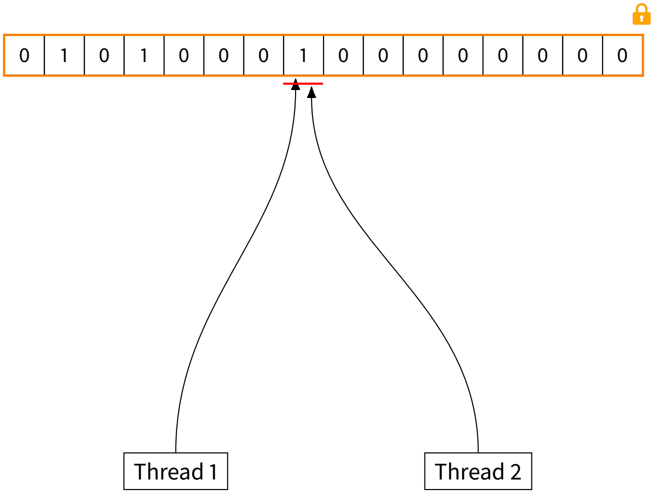

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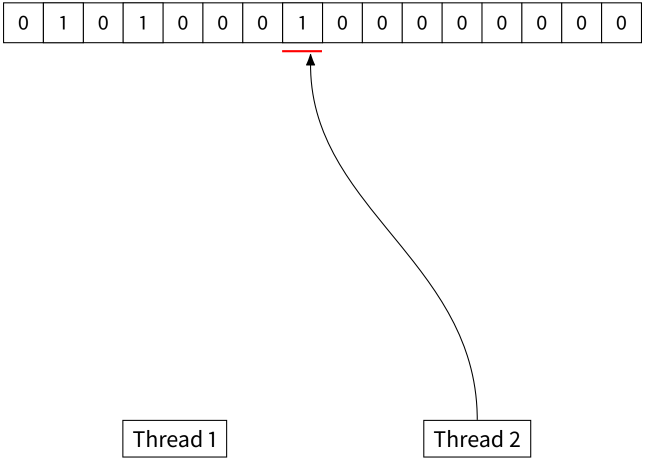

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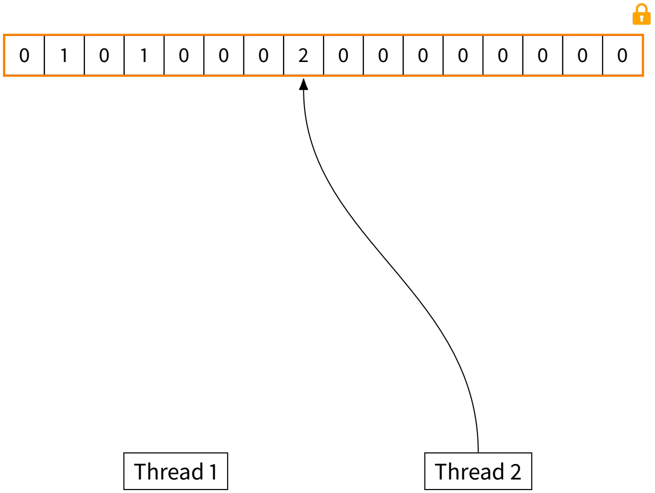


Motivation

Coarse Locking

Unfortunately, coarse-grained locking does not scale!

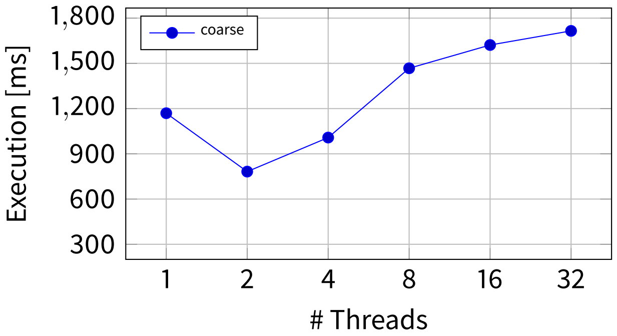


Figure 1: Time to access a shared data structure using coarse-grained locks.

Motivation
Fine Locking

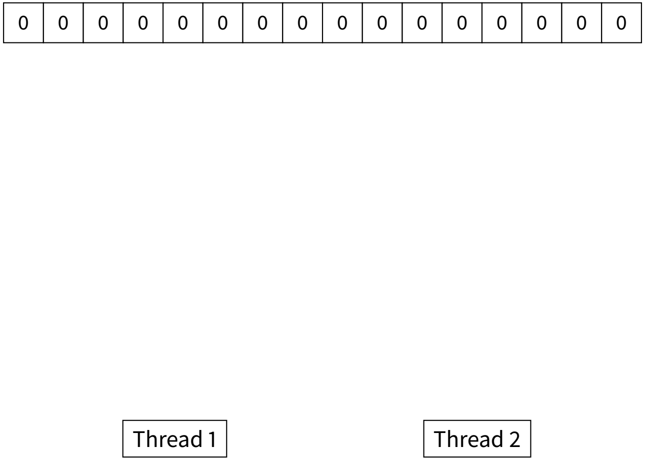
```
int data[SIZE];
std::mutex mtx[SIZE];

void thread_fn(int cnt) {
    /* initialize random */

    for (int i = 0; i < cnt; ++i) {
        auto pos = rand();

        mtx[pos].lock();
        data[pos]++;
        mtx[pos].unlock();
    }
}
```

Motivation
Fine Locking



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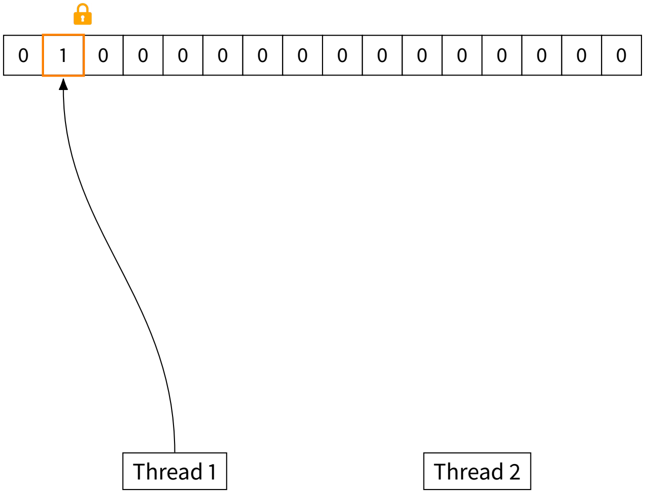

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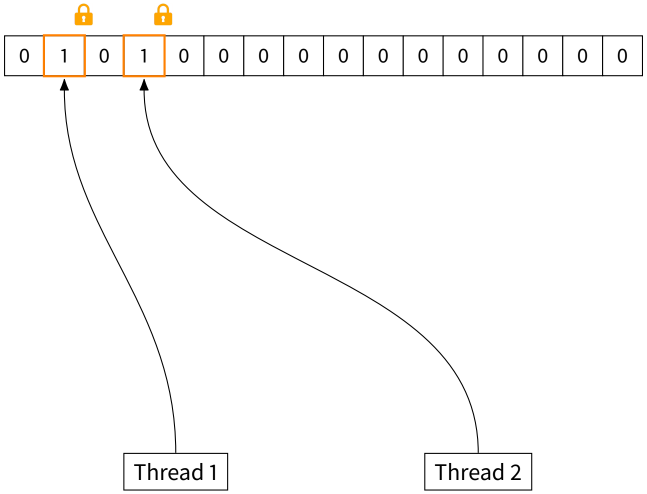

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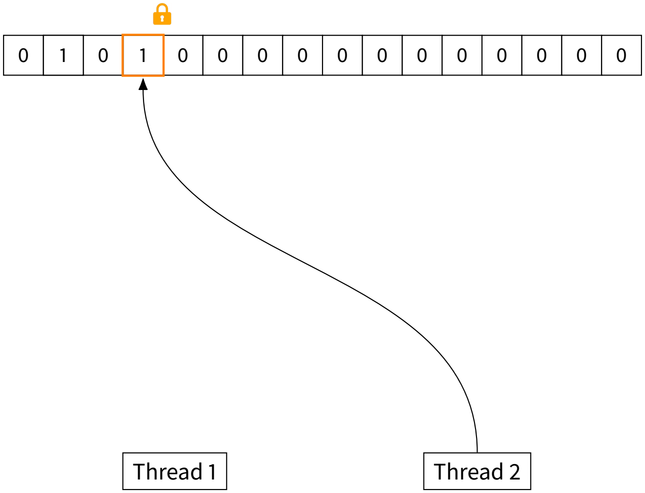

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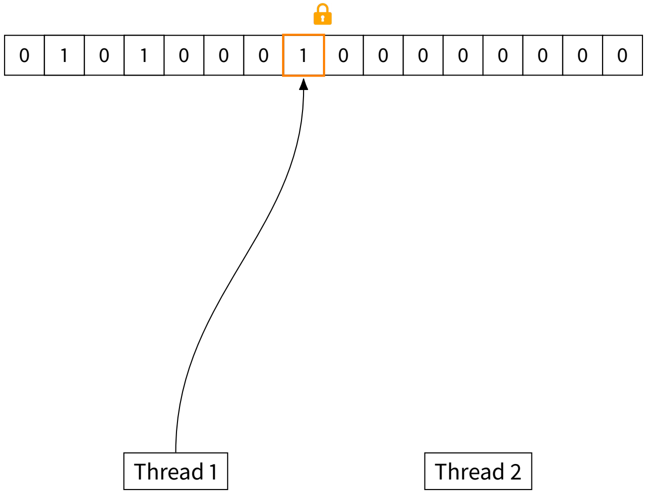

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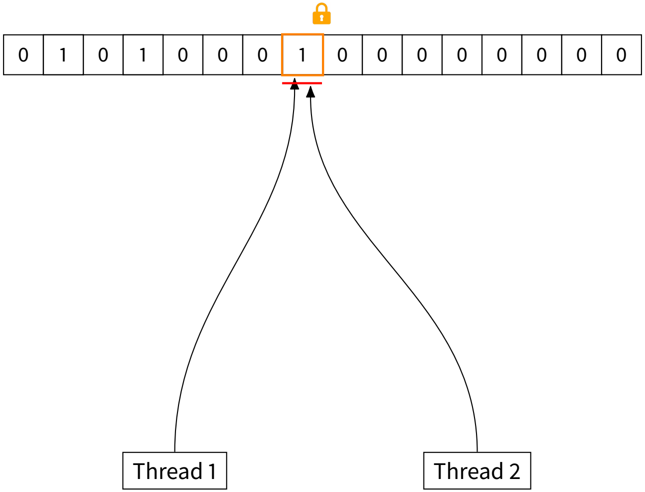

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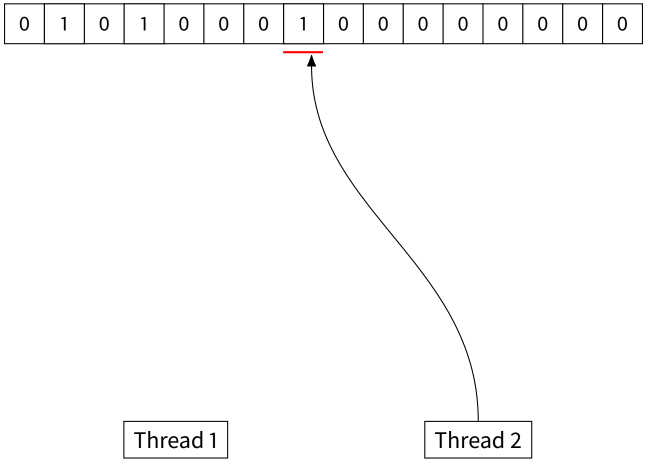

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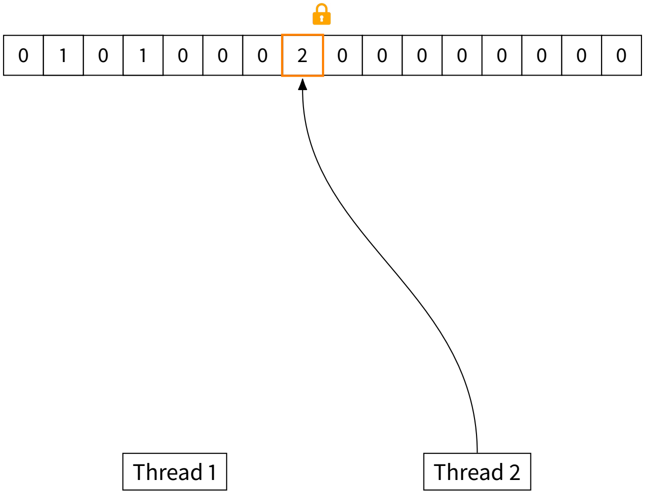


Motivation
Fine Locking

Fine-grained locks scale much better.

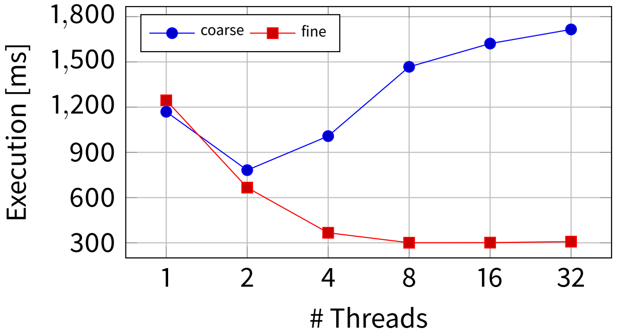


Figure 2: Time to access a shared data structure using coarse-grained or fine-grained locks.

Motivation

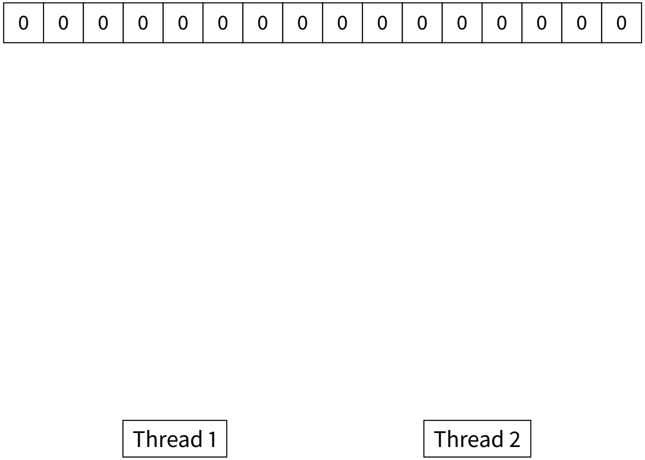
Fine Locking – Deadlock

Fine-grained locks become difficult if multiple locked elements have to be accessed.

```
int data[SIZE];
std::mutex mtx[SIZE];

void thread_fn(int cnt) {
    /* initialize random */

    for (int i = 0; i < cnt; ++i) {
        auto pos1 = rand(), pos2 = rand();

        mtx[pos1].lock();
        mtx[pos2].lock();
        data[pos1] = 2*(data[pos2] + 1);
        mtx[pos2].unlock();
        mtx[pos1].unlock();
    }
}
```

Motivation

Fine Locking – Deadlock



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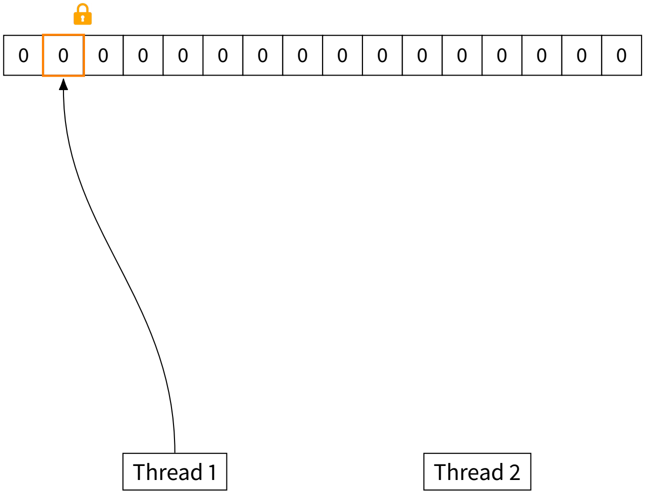

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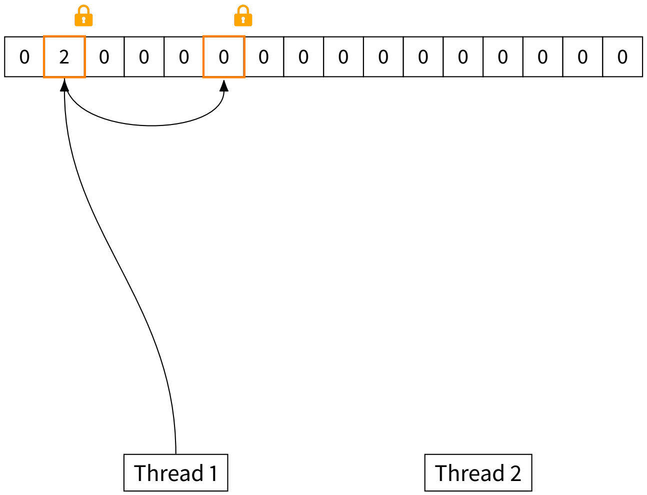

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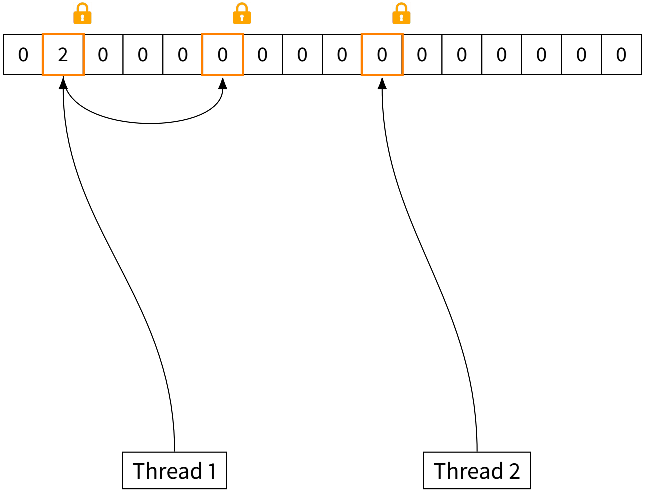

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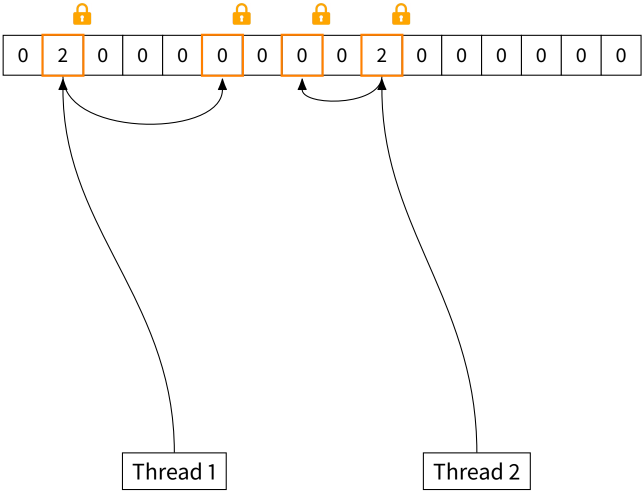

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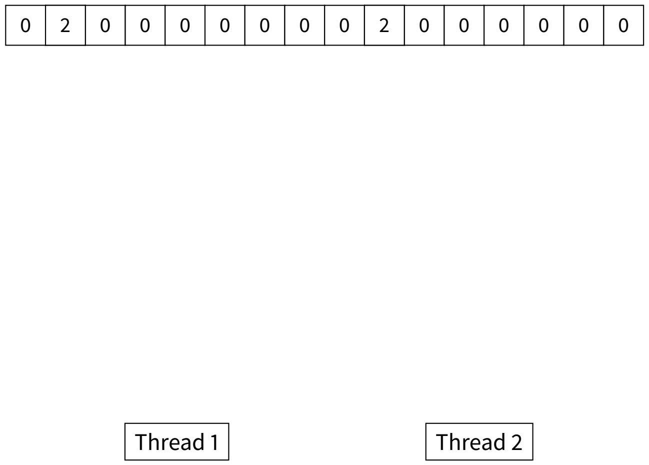

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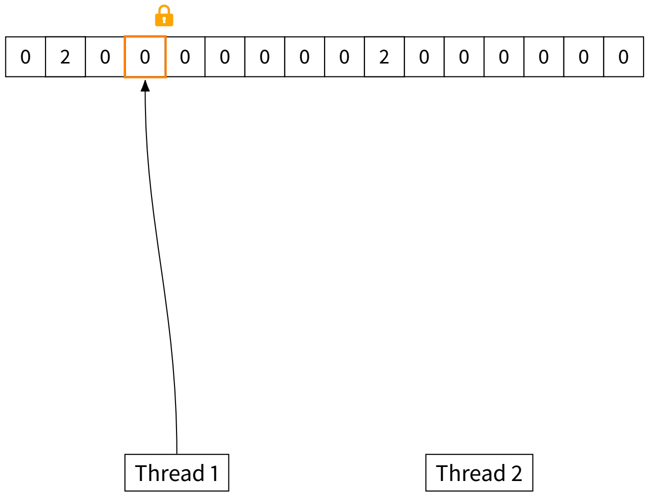

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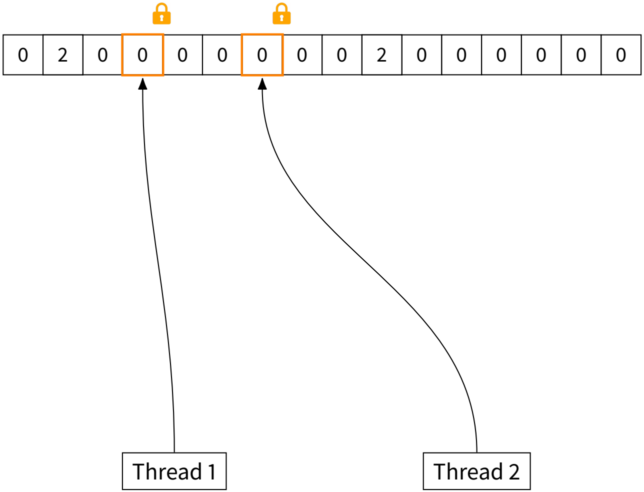

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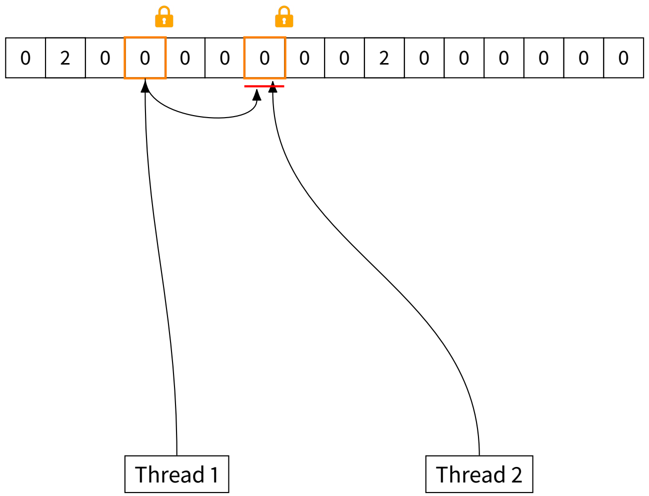

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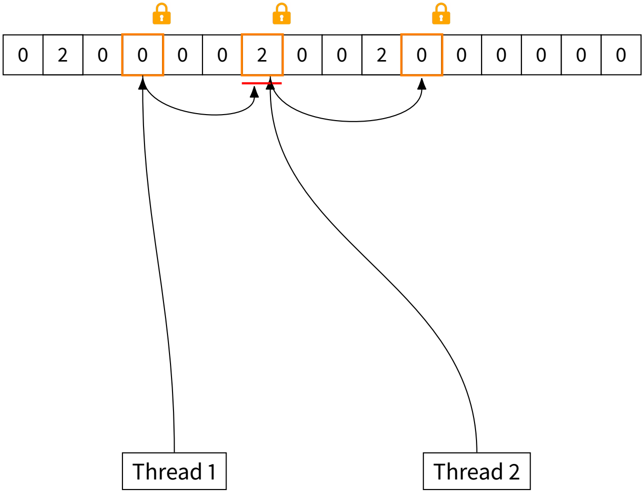

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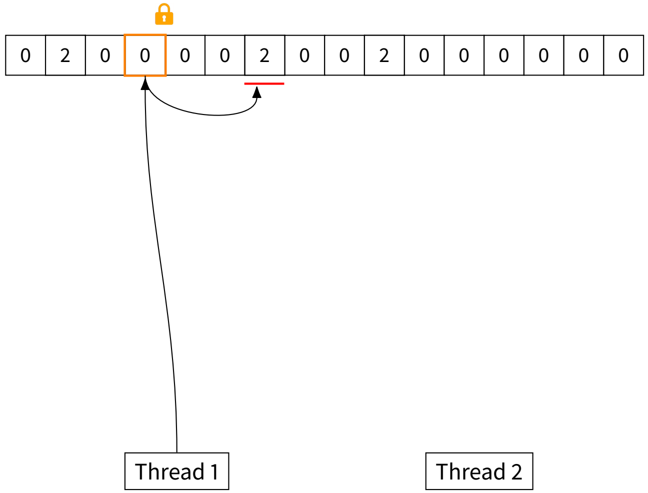

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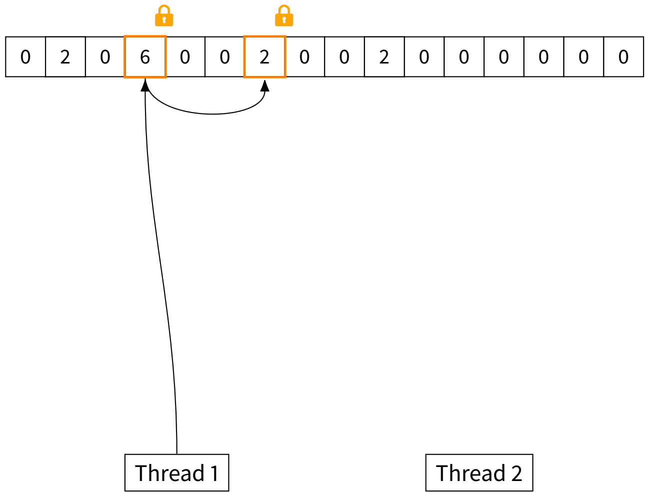

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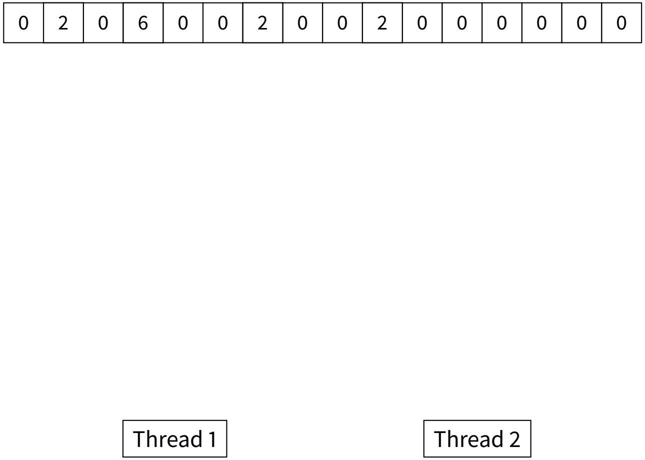

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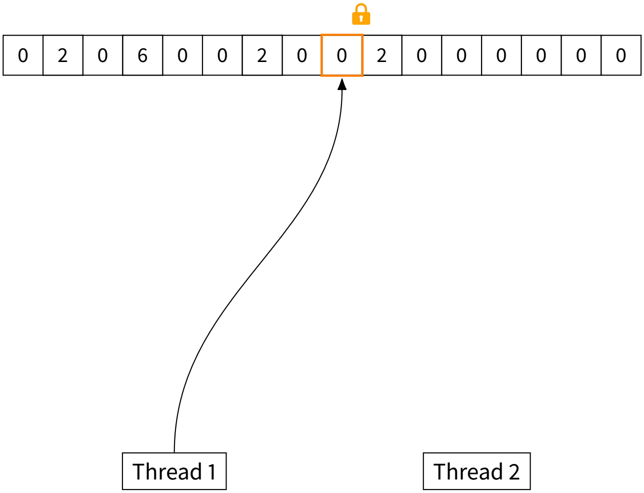

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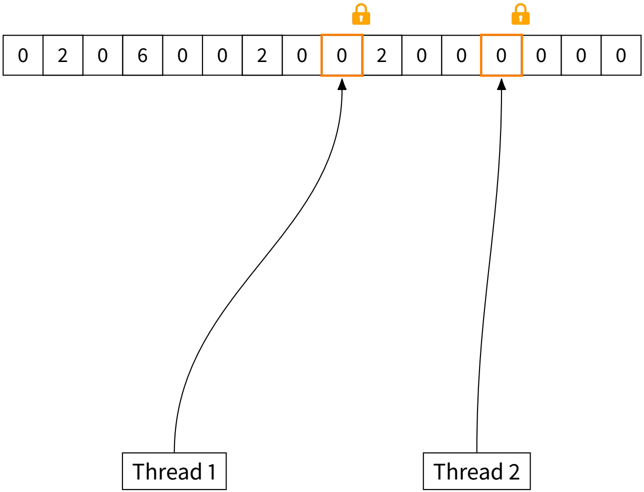

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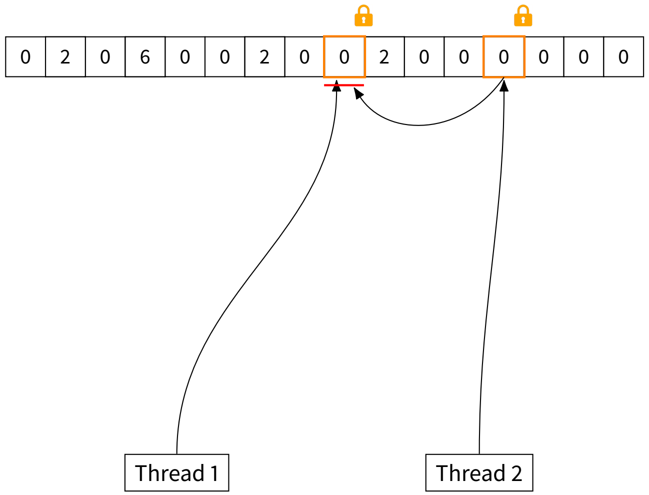

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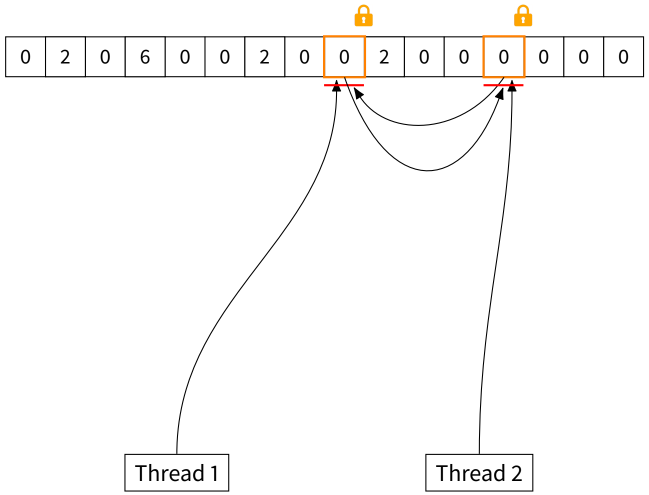

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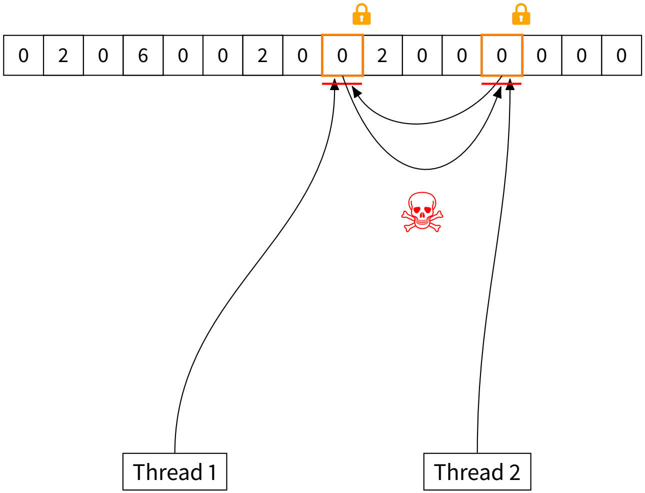

Motivation

Coarse Locks

+ easy to use
+ no deadlock problem
– do not scale well

Fine Locks

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Coarse Locks

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Fine Locks

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Transactional Memory tries to combine the advantages of coarse- and fine-grained locks without having their disadvantages.

Motivation

Transactional memory can provide a similar performance as fine-grained locking.

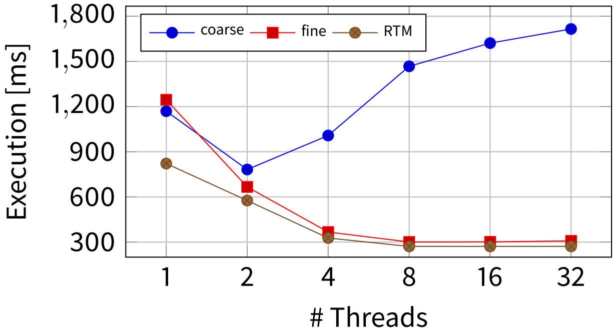

Figure 3: Time to access a shared data structure using coarse-grained locks, fine-grained locks or transactional memory.

Outline

Transactional Memory

Transactional memory provides strong *automicity* and *isolation* guaranties for a finite number of instructions.

Transactional Memory

Transactional memory provides strong *automicity* and *isolation* guaranties for a finite number of instructions.

```
begin_transaction();
/*
 *
 * Critical Section
 *
 *
 */
commit_transaction();
```

- Transactions are started and committed by the programmer.

Transactional Memory

Transactional memory provides strong *automicity* and *isolation* guaranties for a finite number of instructions.

```
begin_transaction();
/* transactional read */
int bar = foo;




commit_transaction();
```

- Transactions are started and committed by the programmer.
- Reads from shared variables are tracked in the *read set*.

Transactional Memory

Transactional memory provides strong *automicity* and *isolation* guaranties for a finite number of instructions.

```
begin_transaction();
int bar = foo;
/* transactional write */
baz = bar * 2 - foo;



commit_transaction();
```

- Transactions are started and committed by the programmer.
- Reads from shared variables are tracked in the *read set*.
- Writes to shared variables are tracked in the *write set*.

Transactional Memory

Transactional memory provides strong *automicity* and *isolation* guaranties for a finite number of instructions.

```
begin_transaction();
int bar = foo;
baz = bar * 2 - foo;
/* explicit abort */
if (bar == 0)
    abort_transaction();

commit_transaction();
```

- Transactions are started and committed by the programmer.
- Reads from shared variables are tracked in the *read set*.
- Writes to shared variables are tracked in the *write set*.
- Transactions can be aborted explicitly.

Transactional Memory

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```
begin_transaction();
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commit_transaction();
```

- Transactions are started and committed by the programmer.
- Reads from shared variables are tracked in the *read set*.
- Writes to shared variables are tracked in the *write set*.
- Transactions can be aborted explicitly.
- Write-write and read-write conflicts are detected by the system.

Transactional Memory

Transactional memory implementations can have many different properties.

Transactional Memory

Transactional memory implementations can have many different properties.

- eager vs. lazy conflict detection

eager	Detect conflicts during the execution of the transaction.
lazy	Check during the commit operation if a conflict happened.

Transactional Memory

Transactional memory implementations can have many different properties.

- eager vs. lazy conflict detection
- undo log vs. write buffering vs. versioning

undo log	Directly write-through to memory and keep log.
buffering	Keep all writes in local buffer and write to memory during commit.
versioning	Maintain multiple versions of the same variable for each transaction.

Transactional Memory

Transactional memory implementations can have many different properties.

- eager vs. lazy conflict detection
- undo log vs. write buffering vs. versioning
- implicit vs. explicit transaction begin

implicit	Automatically start a transaction with the first transactional operation (read, write).
explicit	Only start a transaction at the occurrence of a special operation.

Transactional Memory

Transactional memory implementations can have many different properties.

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- implicit vs. explicit transaction begin
- conflict detection granularity (variables, pages, cache lines, ...)

Transactional Memory

Transactional memory implementations can have many different properties.

- eager vs. lazy conflict detection
- undo log vs. write buffering vs. versioning
- implicit vs. explicit transaction begin
- conflict detection granularity (variables, pages, cache lines, . . .)
- best-effort vs. progress guaranty

best-effort	No guaranty is given which transaction is aborted at a conflict.
progress guaranty	Some guaranties are provided by the system about which transaction is aborted at a conflict.

Transactional Memory

Transactional memory implementations can have many different properties.

- eager vs. lazy conflict detection
- undo log vs. write buffering vs. versioning
- implicit vs. explicit transaction begin
- conflict detection granularity (variables, pages, cache lines, …)
- best-effort vs. progress guaranty
- real nesting vs. flattened nesting vs. no nesting

real	Nested transactions are treated as full-fledged transactions and can commit and abort independently.
flattened	Nested transactions are only virtual transactions. They commit and abort with the surrounding transaction.

Outline

Transactional Memory

Hardware Transactional Memory

- Herlihy and Moss
- IBM Blue Gene/Q and System z
- Intel TSX

Software Transactional Memory

Herlihy and Moss

Hardware Transactional Memory
Herlihy and Moss

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Their idea was to integrate TM support into the processor

Hardware Transactional Memory

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- Special transactional read- and write-instructions

`LT`	Transactionally read the value of a shared variable.
`LTX`	Same as `LT` but with an additional hint a write will follow soon.
`ST`	Tentatively write a value to a shared variable.

Hardware Transactional Memory

Herlihy and Moss

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Their idea was to integrate TM support into the processor

- Special transactional read- and write-instructions
- Special instructions to manage the transaction state

`COMMIT`	Finishes the currently running transaction.
`VALIDATE`	Check if the system detected a conflict with a different transaction.
`ABORT`	Abort the current transaction.

Hardware Transactional Memory
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- Special transactional read- and write-instructions
- Special instructions to manage the transaction state
- Transactions are implicitly started by a transactional read- or write-instruction.
- Conflict detection is done eagerly but aborts must be done explicitly.
- Transactions can contain non-transactional operations.

Hardware Transactional Memory

Herlihy and Moss – Implementation

The cache-coherency protocol is used to detect conflicts between transactions.

Hardware Transactional Memory

Herlihy and Moss – Implementation

The cache-coherency protocol is used to detect conflicts between transactions.

- Cache lines in the *read set* (`LT`) must not be in the *Invalid* state.

Hardware Transactional Memory

Herlihy and Moss – Implementation

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Hardware Transactional Memory

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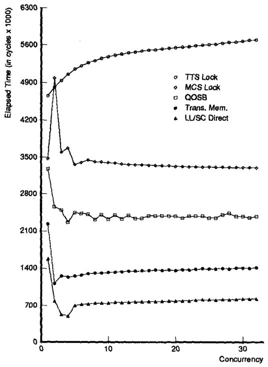
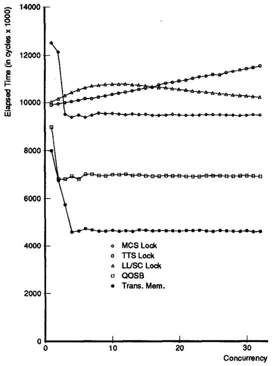
Hardware Transactional Memory
Herlihy and Moss – Results



(a) Counting Benchmark



(b) Double-Linked List Benchmark

Figure 4: Performance results of the H&M-HTM implementation in the *Counting Benchmark* (a) and *Double-Linked List Benchmark* (b).

IBM Blue Gene/Q and System z

Hardware Transactional Memory
IBM System z

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`TBEGIN`	Start a new best-effort transaction, potentially nested.
`TEND`	Commit the currently running transaction.
`TABORT`	Explicitly abort the current transaction.

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- Non-recoverable instructions (e.g. IO), interrupts, and faults also trigger aborts.

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- Filtering of interrupts to prevent switches into the kernel at an interrupt occurrence while being in a transaction.

Hardware Transactional Memory

IBM System z – Results

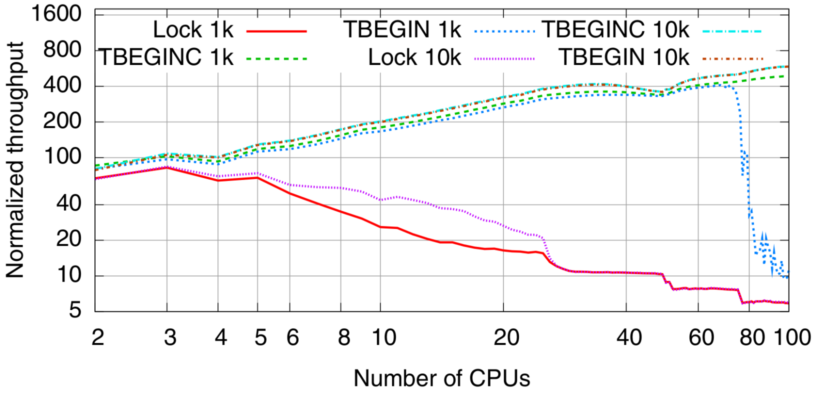

Figure 5: Performance results of the IBM System z HTM when accessing four variables from a pool with 1k/10k elements.

Hardware Transactional Memory

IBM System z – Results

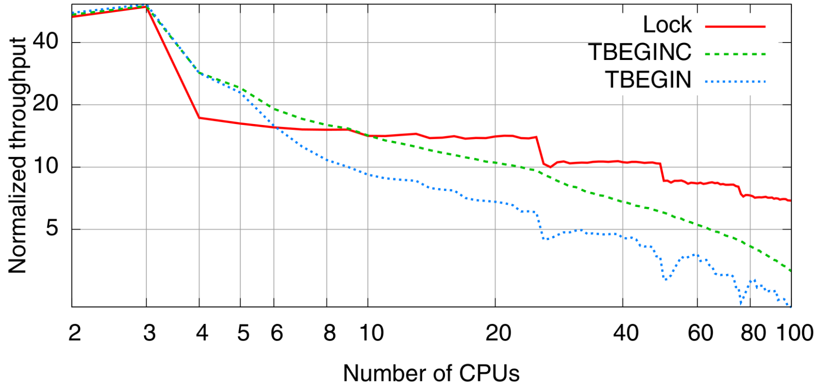

Figure 6: Performance results of the IBM System z HTM when accessing <u>four variables</u> from a pool with <u>10 elements</u>.

Hardware Transactional Memory

IBM System z – Results

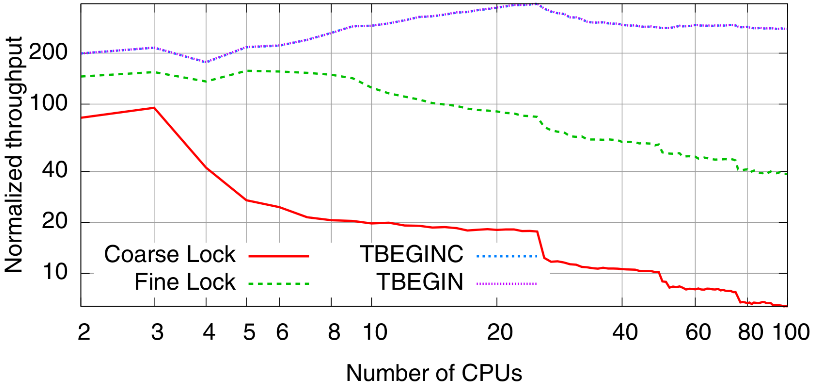

Figure 7: Performance results of the IBM System z HTM when accessing one variable from a pool with 10 elements.

Hardware Transactional Memory
IBM Blue Gene/Q

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IBM Blue Gene/Q

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The Blue Gene/Q HTM additionally provides compiler support and a specialized runtime.

- Software support for transaction retrying and forward progress guaranty.
- Automatic fallback to using locks
- Compiler extensions allowing easy integration of transactional code segments.

```
void thread_fn(int cnt) {
    /* initialize random */
    for (int i = 0; i < cnt; ++i) {
        auto pos = rand();
        #pragma tm_atomic {
            data[pos]++;
        }
    }
}
```

Hardware Transactional Memory

IBM Blue Gene/Q – Results

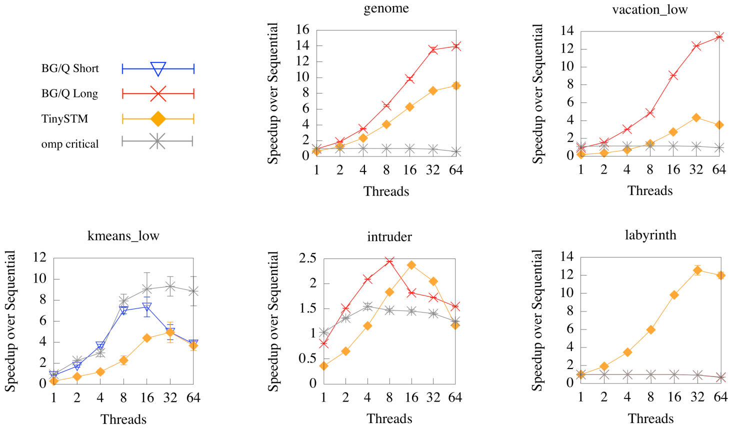

Figure 8: Performance results of the IBM Blue Gene/Q HTM for various benchmarks of the STAMP [10] suite.

Intel Transactional Synchronization Extension

Hardware Transactional Memory

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  - Full featured best-effort transactional memory implementation.
  - Not backward compatible to older processors.

Hardware Transactional Memory
Intel TSX – HLE

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- If the transaction aborts, the CPU will automatically retry and take the lock.
- Older processors ignore the prefix and directly acquire the lock.

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- Interrupts, irrecoverable operations, and faults also trigger aborts.

Hardware Transactional Memory

Intel TSX – Example

```
int data[SIZE];

void thread_fn(int cnt) {
    /* initialize random */

    for (int i = 0; i < cnt; ++i) {
        auto pos = rand();

        while (true) {
            if (_xbegin() == _XBEGIN_STARTED) {
                data[pos]++;
                _xend();
                break;
            }
        }
    }
}
```

Hardware Transactional Memory

Intel TSX – Results

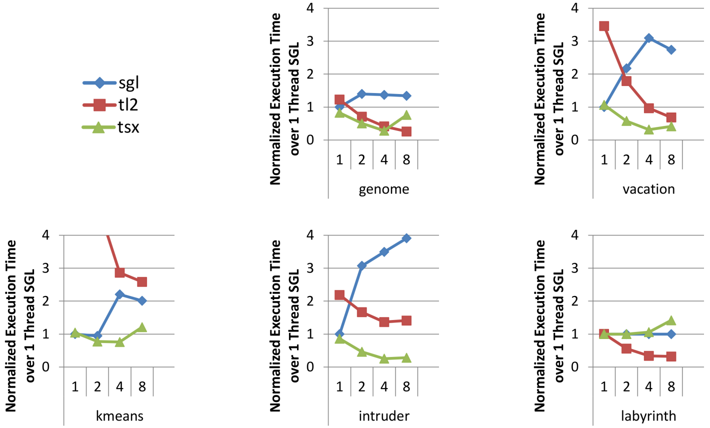

Figure 9: Performance results of the Intel HTM for various benchmarks of the STAMP [10] suite.

Outline

Software Transactional Memory

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Many different implementations of STM exist [5, 7, 1, 2] whereas their performance differs significantly [3, 4].

Any Questions?

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Assignments

Available Topics:

- Distributed Resource Management – Michael
- Transactional Memory – Till
- Robustness in File Systems – Carsten
- Trusted Execution Environments – Carsten/Michael
- Architecture Simulation – Matthias
- Resilince and Fault Tolerance – Matthias
- UNIX-like Systems – Nils
- Distributed Debugging – Maksym
- Performance Modeling – Maksym
- Attacks on SGX – Jan
- HPC vs. Cloud Computing – Jan