On the Integration of DSP Hardware into a Microkernel-based Operating System

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A re-raised Topic

DSPs as accelerators vs. standard CPUs (NSP, MMX, ...)

- Architectural advances in standard CPUs
- Microkernel OS Technology

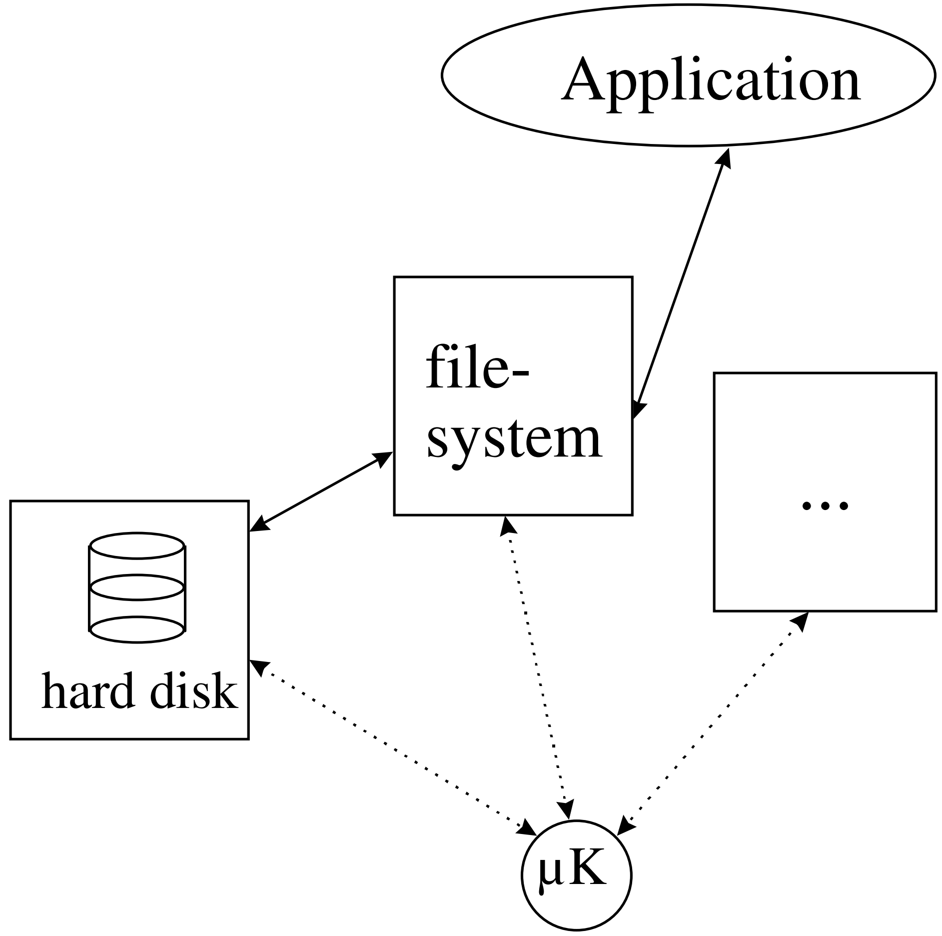
Microkernel-based Operating Systems

small Kernel

- message passing
- processes
- memory management

other OS functionality and applications
as user-level tasks:

- filesystem
- device drivers
- ...
- JPEG decoder



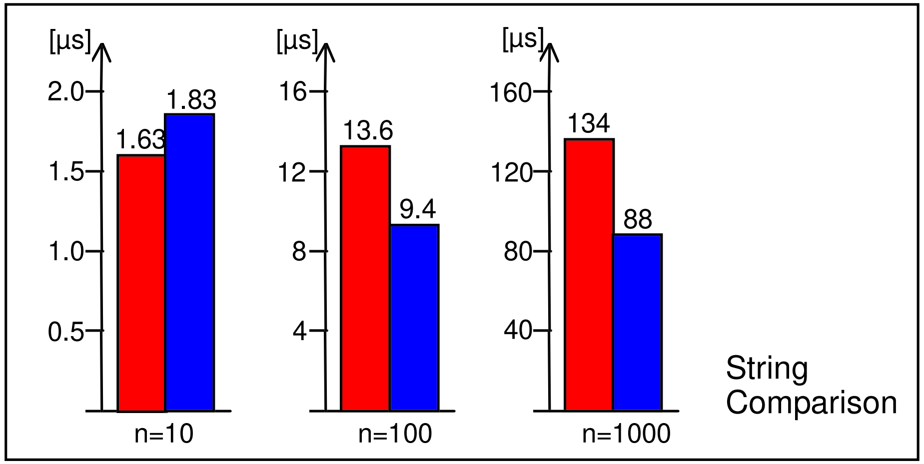
DSPs as Accelerators

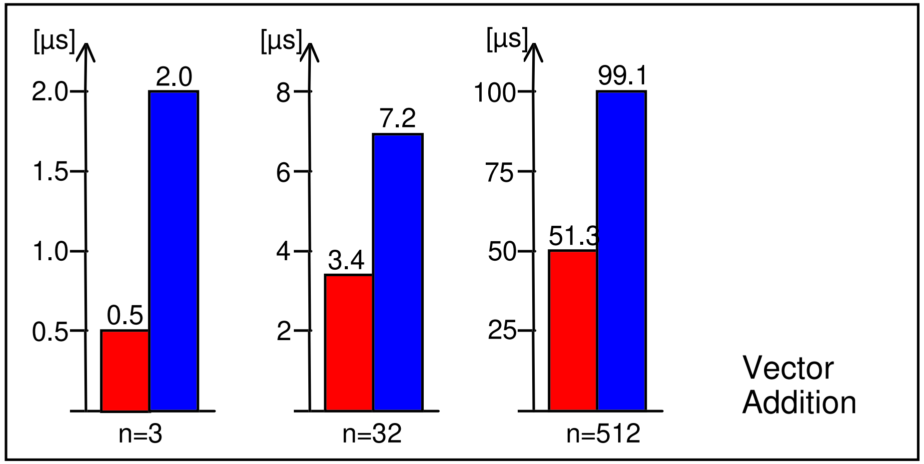
Challenges:

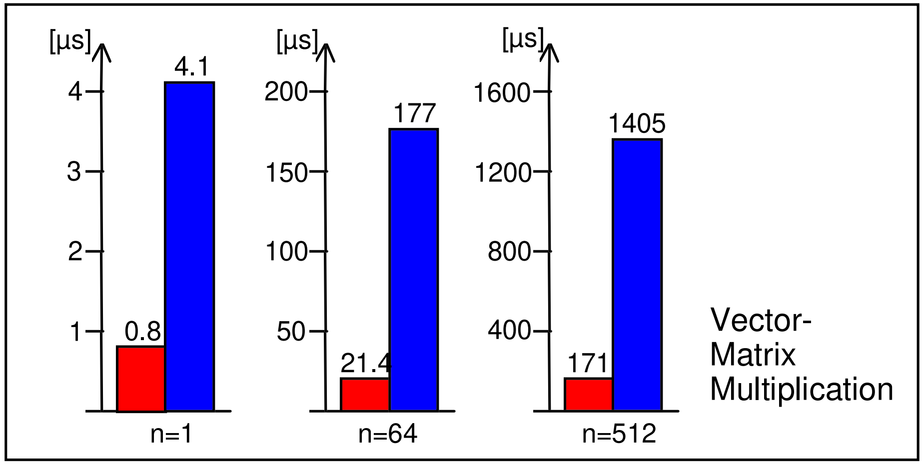
- High overhead by inter-processor communication
- Complex programming model
- Two software development environments necessary
- Inflexible subsystem

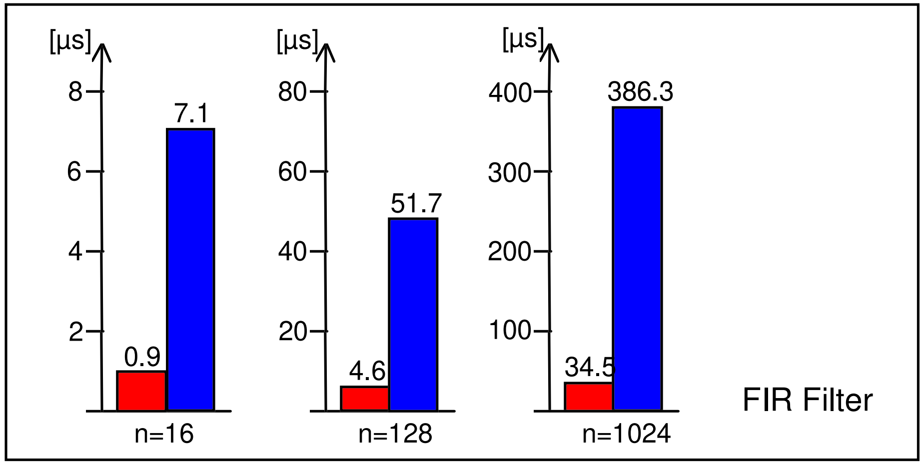
Simple Comparisons

between Motorola 56001/60 and Intel Pentium 60









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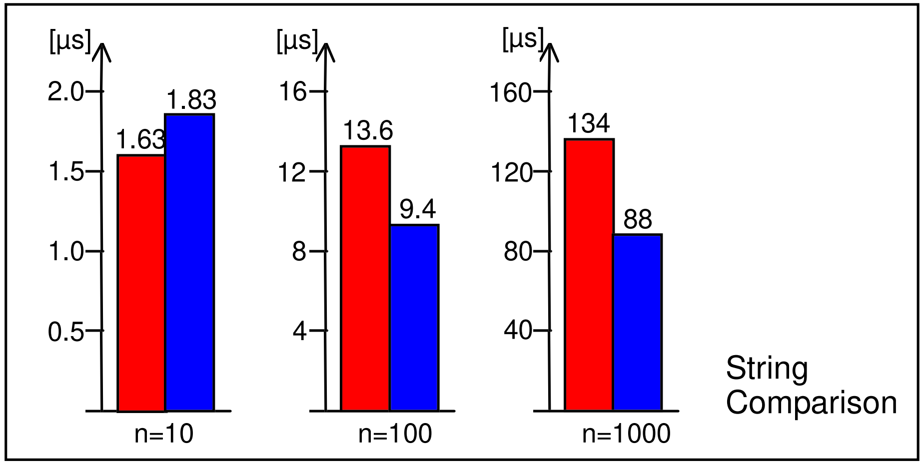
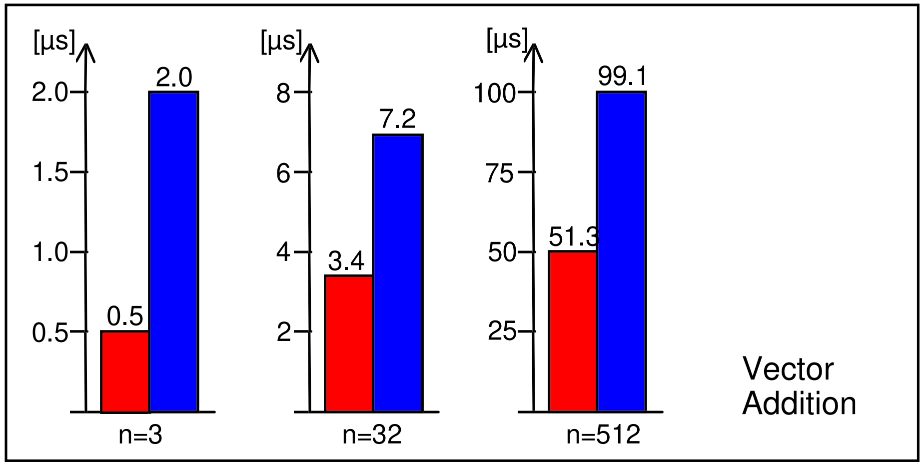
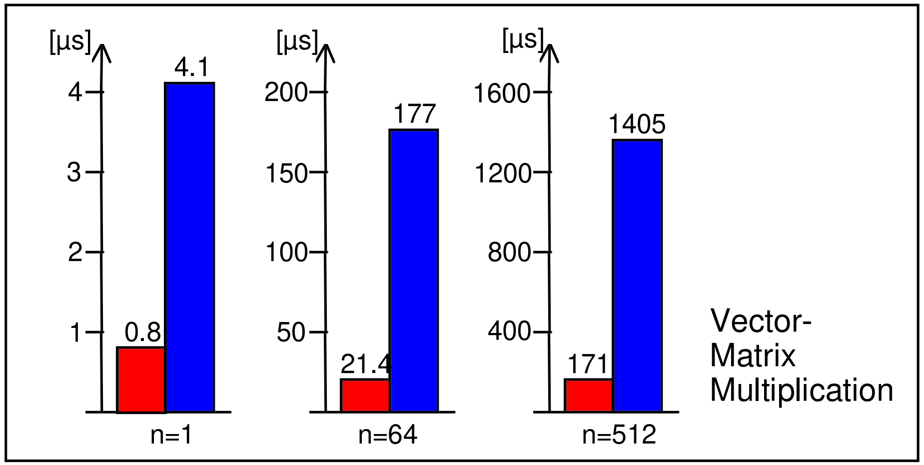
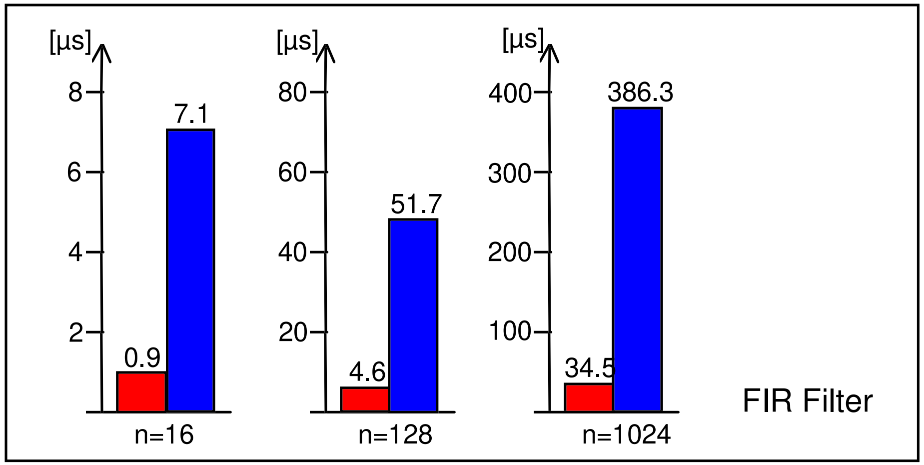

[μs]
2.0
1.5
1.0
0.5
1.63
1.83
n=10
[μs]
16
12
8
4
13.6
9.4
n=100
[μs]
160
120
80
40
134
88
n=1000
String
Comparison


[µs]
2.0
1.5
1.0
0.5
0.5
2.0
n=3
[µs]
8
6
4
2
3.4
7.2
n=32
[µs]
100
75
50
25
51.3
99.1
n=512
Vector
Addition


[µs]
4
3
2
1
0.8
4.1
n=1
[µs]
200
150
100
50
21.4
177
n=64
[µs]
1600
1200
800
400
171
1405
n=512
Vector-
Matrix
Multiplication


[µs]
8
6
4
2
0.9
7.1
n=16
[µs]
80
60
40
20
4.6
51.7
n=128
[µs]
400
300
200
100
34.5
386.3
n=1024
FIR Filter

Algorithms suited for DSPs

have many	have few
additions, multiplications, convolutions	divisions
fixed-length loops	conditional branches
parallel: arithmetics and transport	number format conversions
fixed data format	

Hardware Basis

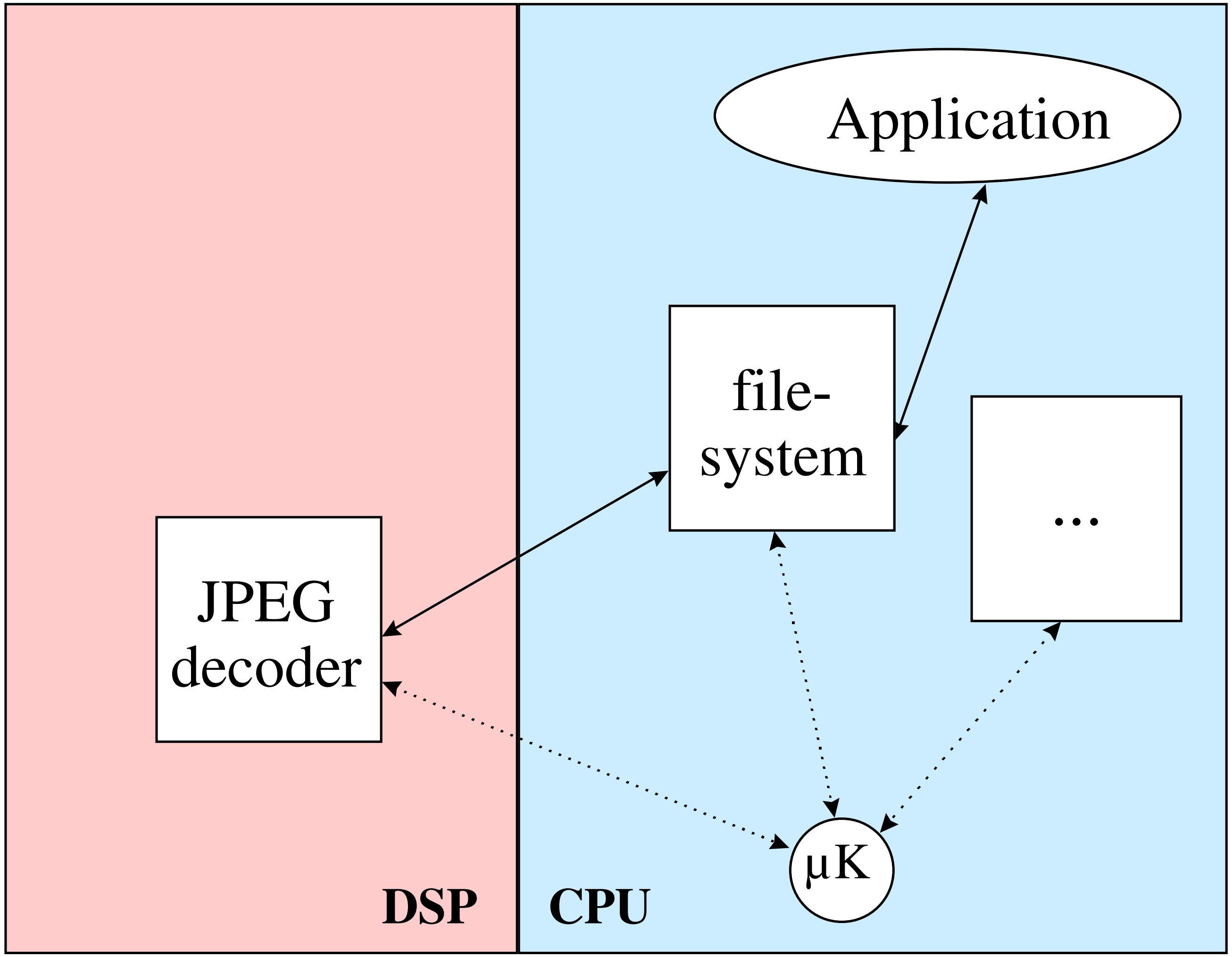
standard PCI PC:

- Intel Pentium , 60 MHz
- 8 MB RAM
- running VSTa µKernel

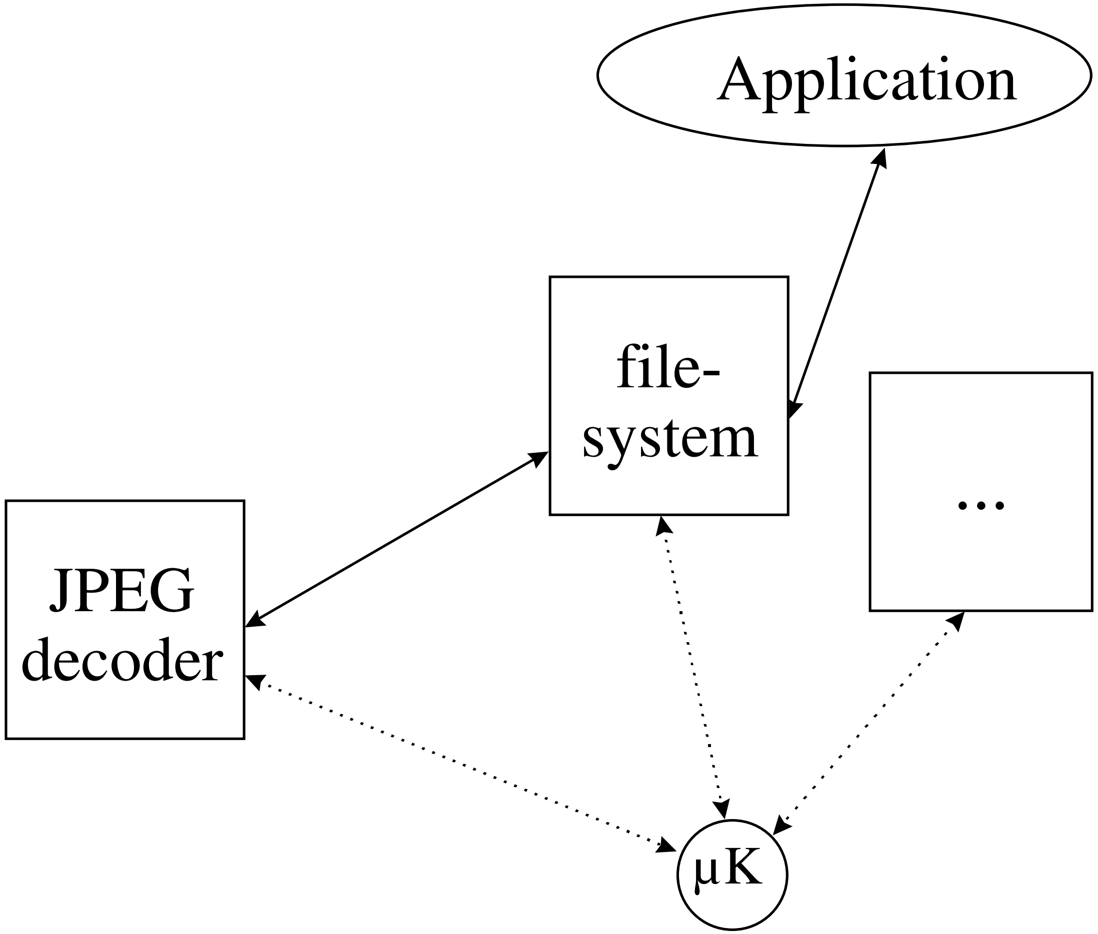
ISA plug-in board (8 bits):

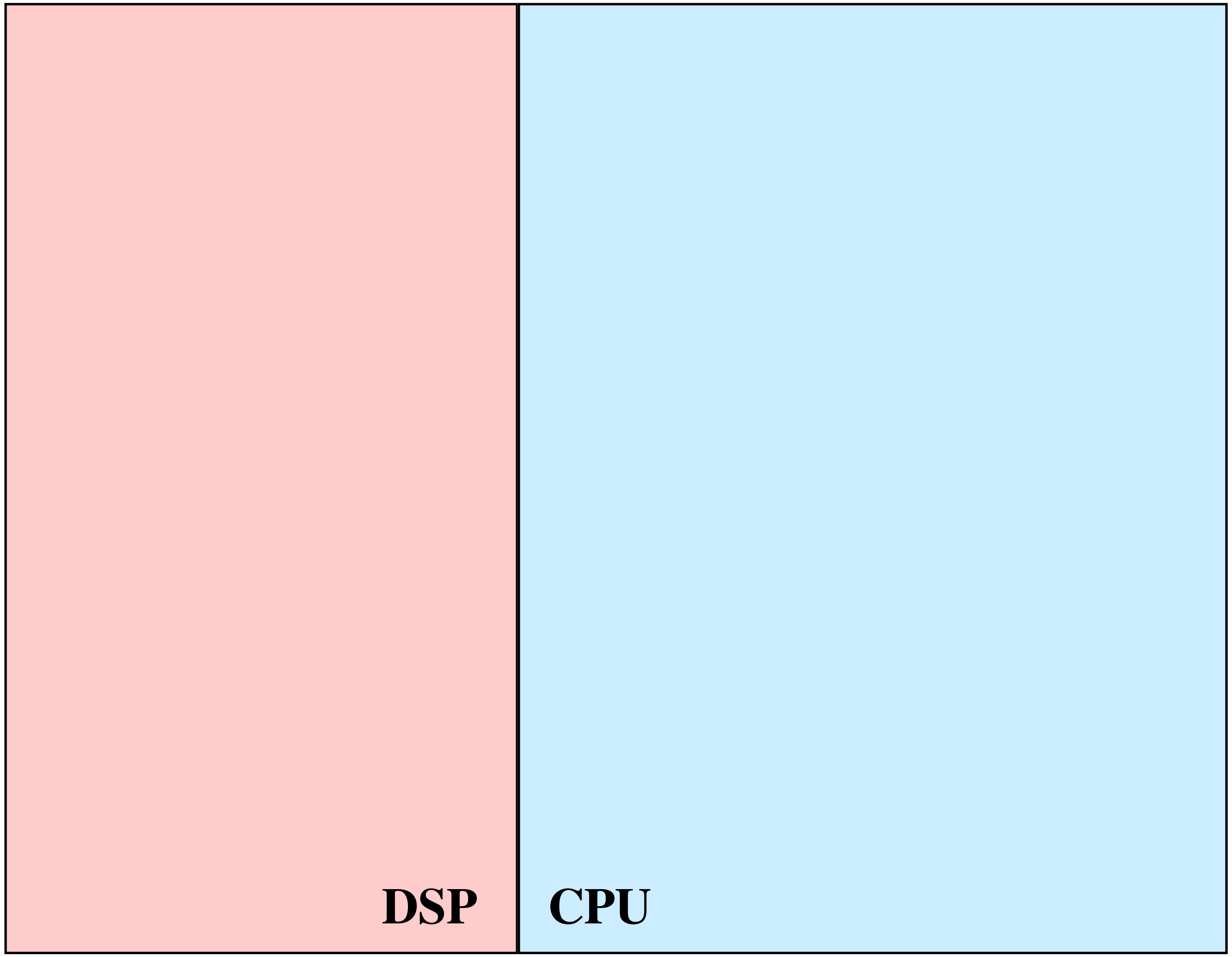
- Motorola DSP 56001, 20 MHz
- 3x32 kWords SRAM

A complex Example



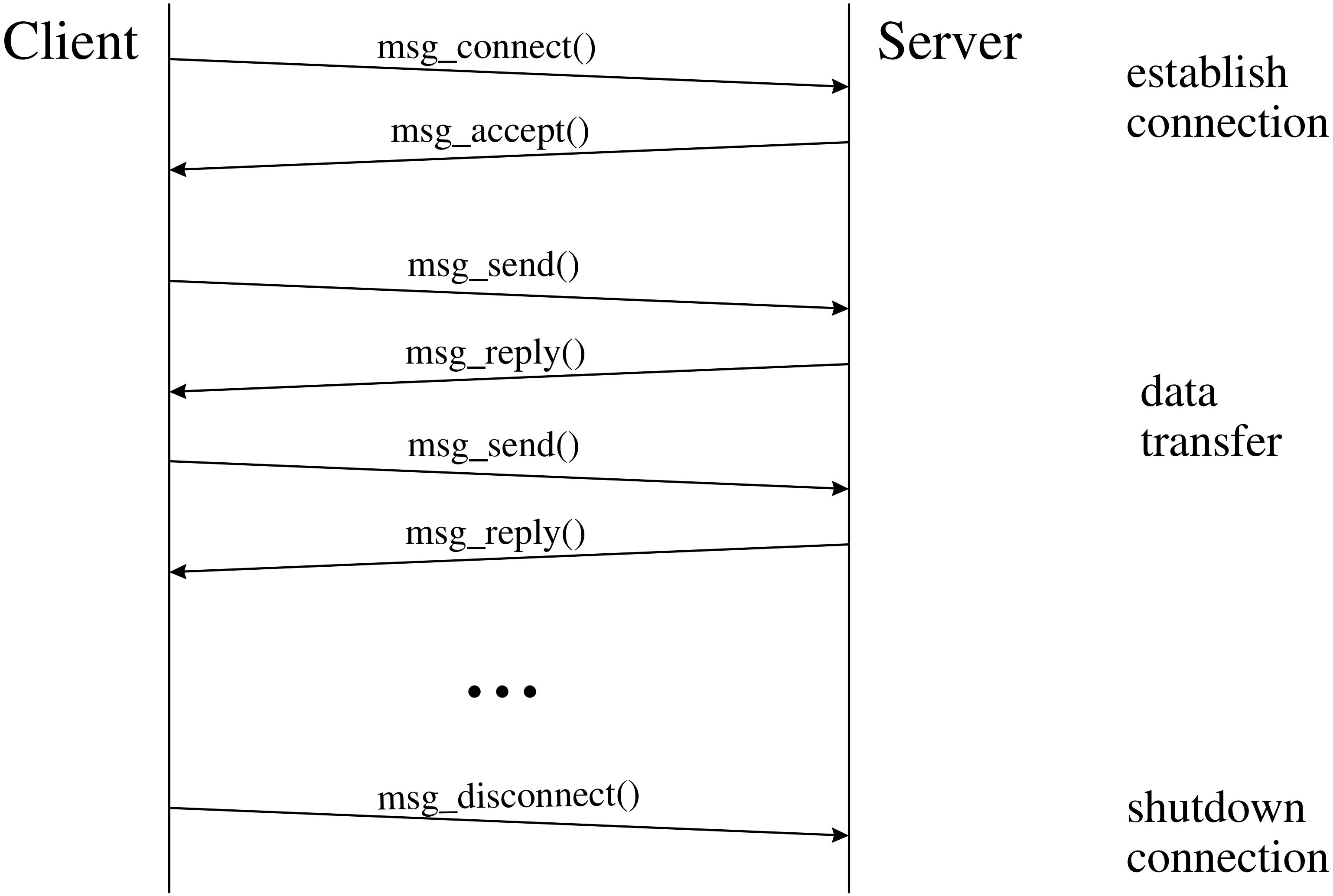
A complex Example




DSP
CPU


CPU

IPC in VSTa

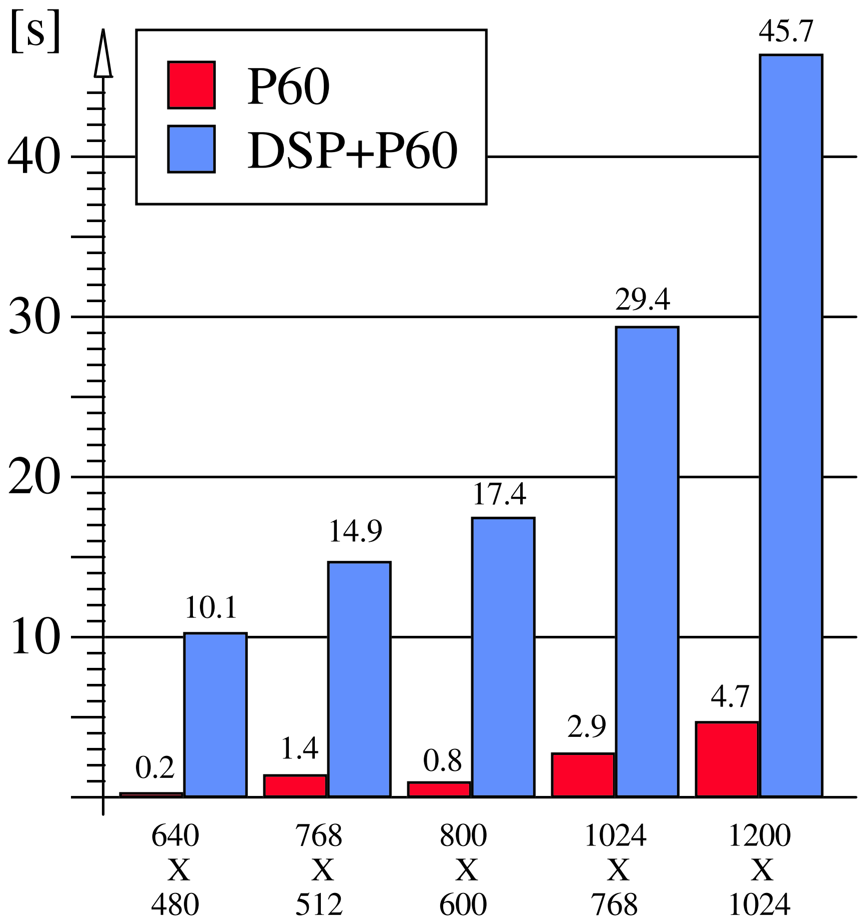

Client
Server
msg_connect()
msg_accept()
msg_send()
msg_reply()
msg_send()
msg_reply()
• • •
msg_disconnect()
establish connection
data transfer
shutdown connection

Results

times per decoded picture:

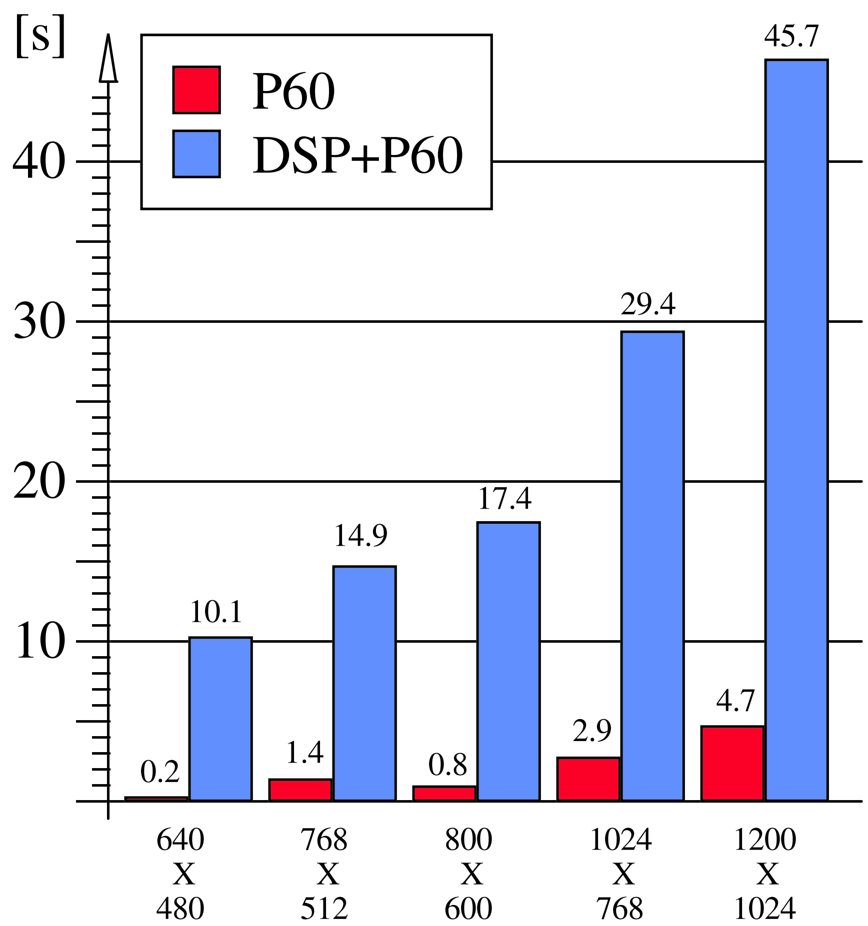
disappointing at first glance

but...



Results

times per decoded picture:



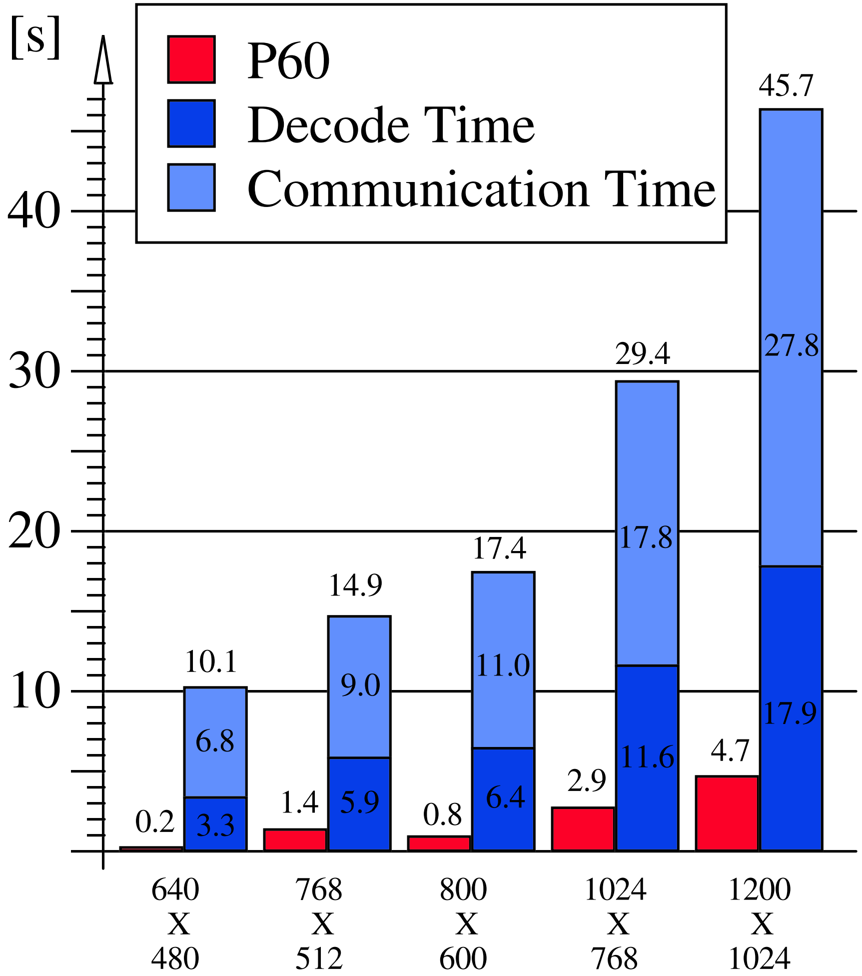
disappointing at first glance

but...

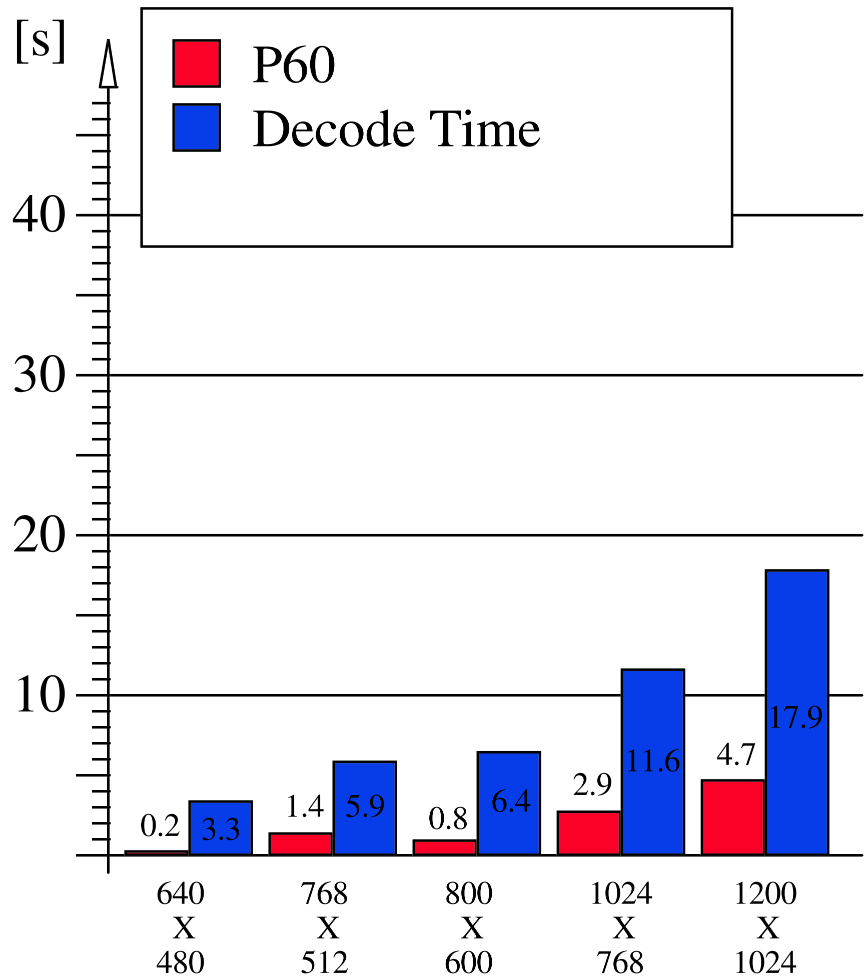
Communication vs. Decode Time

DSP time:

- communication: 67%
- processing: 33%



Communication vs. Decode Time



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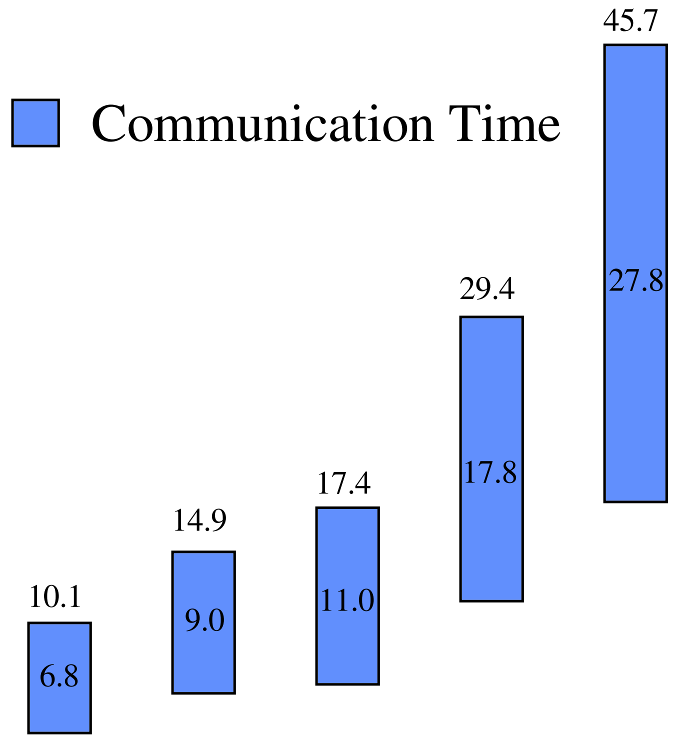

Lessons learned

processing acceptable

communication unacceptably inefficient

The Future

- fast interface between PC and DSP board
- high-speed DSP
- 2nd generation µKernel (L4)

Universal Multimedia Accelerator for PCs