The IMData Approach to Accelerating Data Intensive Workloads

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Abstract. Having started operational work in August 2012, the ESF young researcher group IMData seeks to develop new integrated mechanisms for accelerating data intensive workloads in heterogeneous many-core systems. This extended abstract and the accompanying poster summarizes the observations that motivate the project and the approach we are going to take.

Accelerator architectures such as GPGPUs, IBM Cell, and signal processors achieve their performance and energy advantages by offering a vast number of very simple and specialized cores. The tremendous core count of these architectures stems in part from a sacrifice of even the most fundamental hardware features that interacting applications and operating system kernels require. However, for not frequently interacting workloads, this tradeoff pays off in gigantic speedups.

Comparing different Alpha generations, Kumar et al. [2] already found that little less than five simple cores occupy the same area as a large out-of-order core motivating a combination of few big and many little cores in single-ISA heterogeneous systems. However, the chip area requires to support an operating system suprised us. We configured two Tensilica Xtensa cores [1] for a 400MHz 65nm Low Power Process Technology using the Xtensa Xplorer Tools. One of it is used in the Tomahawk MPSoC accelerator for Software Defined Radio [3]. The other has all features enabled that modern general purpose operating systems require (interrupts, exceptions, ...). Adding OS support to a core (notice, we stick to the same ISA and application-level execution profile) increases the core's area by almost 100% from 0.095 mm^2 to 0.171 mm^2 (excluding caches). Therefore, just by removing hardware support for the operating system, thread parallelism could be doubled. Additionally, replacing the

32 KB tightly coupled SRAM with two 16 KB caches for instructions and data, multiplies chip area by almost another factor of two (from 0.299 mm^2 vs. 0.516 mm^2).

The research direction, which we derive from this obseration is therefore how to enable complex, interactive and data intensive workloads on accelerator platforms without sacrificing the benefits obtained from hardware specialization. The immediate questions that arise are: "How can we control applications without having full hardware support for running an operating system kernel beneath them?", "How can applications on different cores interact with each other?", "How can they synchronize on shared data and communicate results?", "How can critical parts of applications be isolated?", and finally, "How can all this be achieved without reintroducing the area-expensive hardware mechanisms of general purpose architectures?".

At the hardware level, the starting point will be the Tomahawk processor built by TU Dresden's mobile communications group. On top of it, the L4 microkernels NOVA and Fiasco.OC from TUD's operating systems group will provide efficient and light-weight communication and synchronization mechanisms to the data intensive applications, which we draw from in-memory databases and from other research fields of TUD's database and data analytics group. In addition, our probablistic model checking group will support us by looking into new techniques for investigating functional and non-functional properties of our algorithms and system components.

References

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